4.4 A 12.5Gb/s Single-Chip Transceiver for UTP Cables in 0.13µm CMOS

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The use of unshielded twisted pair (UTP) cabling is ubiquitous in many data center applications. However, for extremely high data rates, current choices are fiber-optic solutions or custom cables and connectors. The usability of fiber is limited both by cost and installation difficulties, while current copper solutions suffer limited range, bulky cables, and high power consumption. Further, neither of these solutions can take advantage of existing cable infrastructure. Power consumption is limited for many types of existing 10G fiber modules [1] requiring power consumption below 4W. Additionally, low latency is desirable for many applications. This design has considerably longer reach than existing copper solutions while meeting the stringent power requirements as well as supporting multiple data rates from 5Gb/s up to 12.5Gb/s.

Due to the bandwidth limitations of UTP cabling, this approach utilizes a four-lane full-duplex 4-PAM signaling scheme to reduce the baud rate to between 625MHz to 1.5625GHz. This approach requires echo cancellation, near-end crosstalk (NEXT) cancellation, transmit pre-conditioning, and receive equalization to remove the various system impairments and to compensate for the low pass response of the cable. To reduce power consumption as well as limit latency, the intensive application of adaptive analog FIR filters is used instead of the traditional DSP approach.

Figure 4.4.1 shows a block diagram of the complete transceiver. A low-jitter LC tank VCO creates the system clock at 1.25 to 3.125GHz. This clock is used for both the line and system interfaces. A continuous-time version of a transmit replica canceling hybrid scheme similar to [2] is used to allow full-duplex operation by removing most of the transmit signal from the desired receive signal before entering the receiver.

The input stage of the receiver consists of a programmable transconductance (Gm) stage with an integrated equalizer. The schematic and frequency response are shown in Fig. 4.4.2. The combinations of these circuits and an adaptive DFE achieves line equalization of up to 20dB (at the Nyquist frequency) with small noise emphasis penalties. The input gain is controlled digitally and is set during the startup sequence, providing coarse gain control.

An echo canceller (EC) is included in the receiver to remove echo components that are not cancelled by the hybrid. These echo signals arise from mismatches in the hybrid, discontinuities in the chip package, PCB, connectors, and the cable itself. Due to the large reflection at the connectors, the required span of the EC must be sufficiently long to cancel the reflection caused by the far-end connector.

Another significant source of signal impairment is NEXT, which arises from coupling between channels in the chip package, on the PCB, within connectors, and inside the cable itself. Three NEXT cancellers are included in each channel of the receiver to remove signal components from the neighboring channels that couple onto the receive signal. Again, because of reflections in the connectors, the required span of the NEXT canceller must be sufficiently long to cancel far-end connector reflections.

Included in the receiver is a DFE to remove ISI [3]. To meet settling time requirements, the first tap of the DFE is summed at the input to the hard-decision slicer. The remaining taps are implemented separately to reduce the capacitance on the slicer summing node. Also included with the DFE is a dc-offset correction tap.

All of the filter taps are implemented in a similar fashion as shown in Fig. 4.4.3. Each has an input analog coefficient represented as a differential current. This coefficient is mirrored into small 2b current steering DACs controlled by digital data (either from the transmit data stream for EC and NEXT, or received data for the DFE). Mismatch between the ±1N and ±2N current sources can create distortion. This mismatch is a function of the current source area that sets the minimum physical size of the taps.

At the output of the input Gm stage is a main summing node that subtracts the echo, NEXT, ISI, and dc-offset signals from the received signal. This resulting signal is then sampled by a high-speed track-and-hold. Because the receive data is sampled and has arbitrary phase, a timing-recovery loop is required.

The output current from the track-and-hold feeds a resistive load creating a voltage input to the hard decision slicer. The slicer is composed of three high-speed comparators that slice at the -2h0/0/+2h0 signal levels, where h0 is the signal level of a +1 data pulse. Additionally, two more comparators are used to slice the signal at ±3h0 levels to determine the sign of the signal error that is used in coefficient adaptation. The block diagram of the complete slicer is shown in Fig. 4.4.4. The comparators use an adaptive reference control (ARC) to fine tune the slicer reference levels.

The recovered data and error measurements are used to adapt the various loops that are common in many analog-filter implementations. To ease implementation, the sign of the error is used instead of the error itself, which is a commonly used approximation [3]. The coefficient adaptation pulse for each coefficient is created digitally by multiplying the current sample error signal with a tapped-delay line output containing the transmit data (for the echo canceller and NEXT canceller) or the recovered data (for the DFE and ARC) or a constant (for dc Offset). The adaptation pulse drives a differential analog charge-pump whose output is integrated onto a capacitor. The resulting voltage is converted to a current for use in the taps after being low pass filtered to remove noise. An analog integrator and coefficient generator allows a much finer resolution of the tap coefficient than could be achieved with digital circuitry for the same power, reducing noise that could become a significant impairment for a receiver containing a large number of taps.

Figure 4.4.5 shows scope traces of the signal at the output of the transmitter for a single channel at a 12.5Gb/s data rate after 1m and 35m of CAT-6 cable. Figure 4.4.6 shows the recovered signal after 25m of CAT-6 cable at 10Gb/s. Note that the eye monitor test path has a bandwidth of 800MHz, which adds significant ISI to the waveform, although the eye is still clearly open.

The transceiver described is implemented in 0.13µm CMOS. The total core die area is 42mm^2 with the die micrograph shown in Fig. 4.4.7. Initial lab measurements show a 30m link at 10Gb/s over CAT-6 cable achieving a BER < 10^{-12} with a power consumption of 4.0W. Lower power consumption is possible for lower bit rate operation or shorter cable lengths.

References:

[1] XENPAK 10 Gigabit Ethernet MSA - Issue 3.0, Sept., 2002.

[2] J. Jaussi, et al, "An 8 Gb/s Source-Synchronous I/O Link with Adaptive Receiver Equalization, Offset Cancellation and Clock Deskew," *ISSCC Dig. Tech. Papers*, pp. 246-247, Feb., 2004.

[3] N Kelly, D Ray, D Vogel, "A Mixed-Signal DFE/FFE Receiver for 100Base-TX Applications," *ISSCC Dig. Tech. Papers*, pp. 310-311, Feb., 2000.

 1-4244-0079-1/06/$20.00

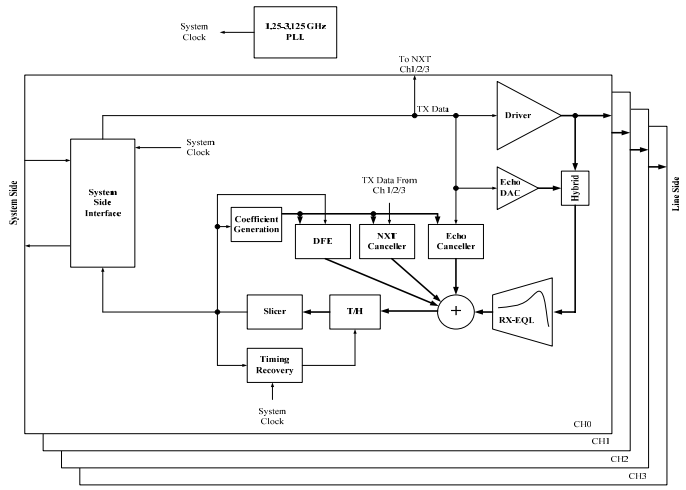

Figure 4.4.1: Chip block diagram.

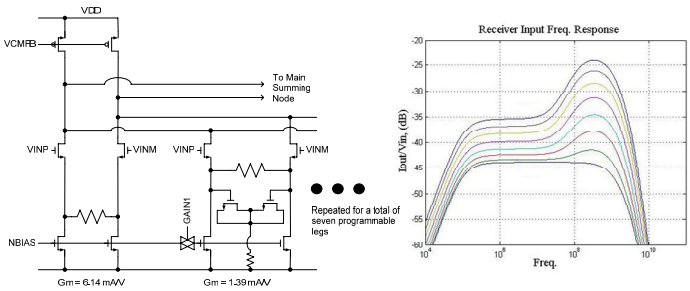

Figure 4.4.2: Receive equalizer.

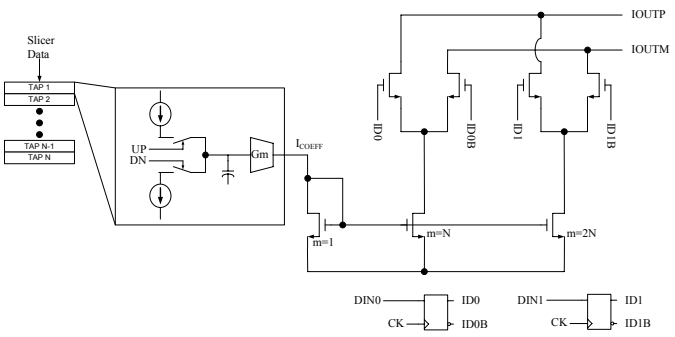

Figure 4.4.3: Coefficient Generation.

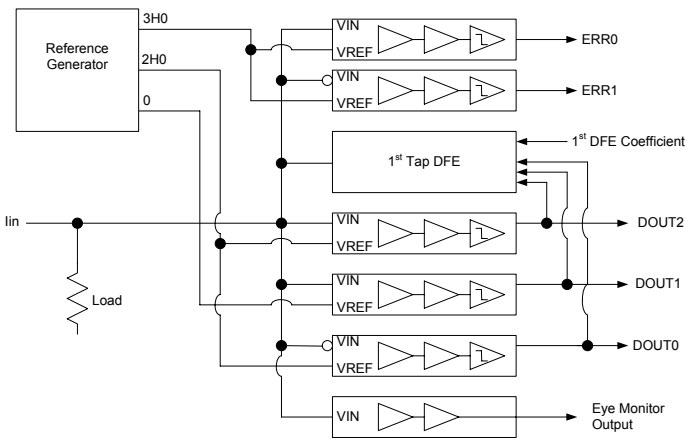

Figure 4.4.4: Slicer block diagram.

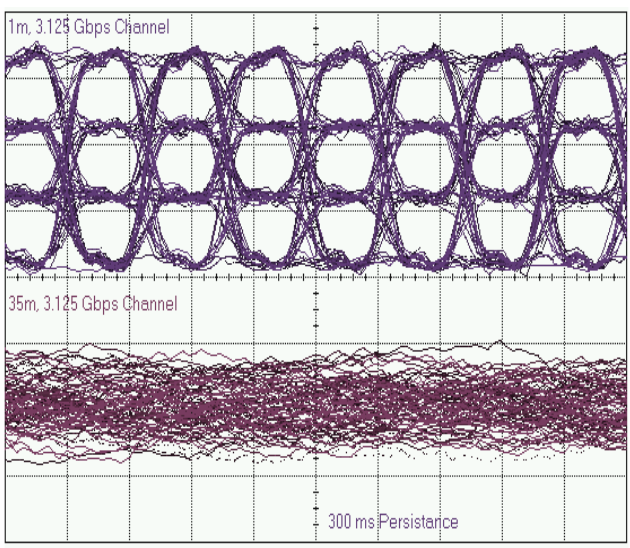

Figure 4.4.5: Transmit eye.

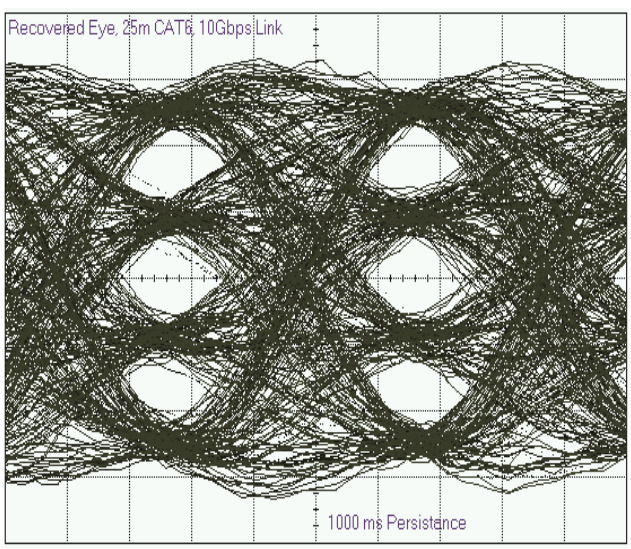

Figure 4.4.6: Receive eye at 25m.

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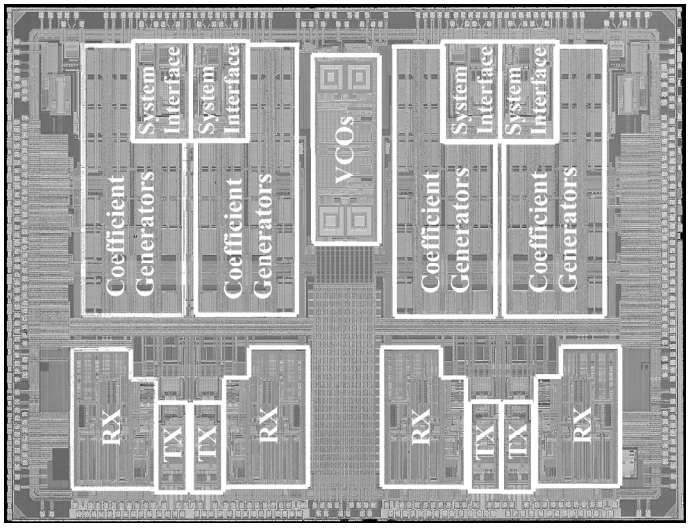

Figure 4.4.7: Die micrograph.

